REMARKS

The Office action of December 23, 2003 has been received and its contents carefully noted.

Claims 1-17 are pending in the application. Claims 16-17 have been added without the addition of any new matter. In accordance with the Action, Claims 2-7, and 9-15 have been amended to include all of the features of the base claim and any intervening claims.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being unpatentable over Yokoyama (U.S. Patent No. 6,014,095). Claim 8 stands rejected under § 102(b) as being unpatentable over Fukuzawa (U.S. Patent No. 5,933,536). Applicant respectfully traverses these rejections, and requests allowance thereof in the continuation prosecution application for the following reasons.

The Claims are Patentable Over the Cited References

Claim 1 is not anticipated by Yokoyama

Claim 1 stands rejected under § 102(b) in view of Yokoyama. Applicants strongly contend that Yokoyama fails to disclose the features recited in these claims such as a run-length converter for converting block data consisting of a plurality of image signals into combined data in accordance with a scanning sequence, each of the combined data including a number of consecutive insignificant coefficients and a value of a significant coefficient next to the consecutive insignificant coefficients.

Yokoyama makes no mention of this feature as in contrast Yokoyama discloses a variable length encoding system that uses a combination of a motion estimator, motion compensation predictor, and a discrete cosine transformer(DCT)/quantizer to determine coefficients for an incoming block of image signals. (see FIG. 4; col. 7, lines 65-67; col. 8, lines 1-23). Specifically, Yokoyama states that "...an image signal is read out from the frame memory 1 in units of a block...next...a motion estimator 2 searches a motion vector in units of one block, and detects a prediction mode and the motion vector...a motion compensating predictor performs a motion compensating interframe prediction on the basis of the detection motion vector and prediction mode...a subtractor 4 calculates a difference...a DCT processing unit 5 orthogonally transforms the difference data...and obtains transform coefficients." (see FIG. 4; col. 7, line 67; col. 8, lines 1-20).

Therefore, Yokoyama does not use a run-length converter to convert block data from an image signal into combined data in accordance with a scanning sequence where the combined data includes a number of consecutive insignificant coefficients and a value of a significant coefficient next to the consecutive insignificant coefficients. In strong contrast, Yokoyama discloses use of a motion estimator, motion compensating predictor, subtractor, and DCT processing unit to obtain coefficients from the input block of image data. Applicant strongly contends that using

a combination of motion estimators/predictors and DCT processors to obtain coefficients from an input block of image signals as disclosed by Yokoyama is significantly different from the recited feature of using a run-length converter to obtain combined data, in accordance with a scanning sequence, including insignificant coefficients and a value of significant coefficients.

Furthermore, as clearly illustrated in FIGs. 5, 6 of the cited reference, Yokoyama teaches away from the recited invention by performing the steps of determining/counting coefficients, storing a variable length code, and performing the variable length coding all within the variable length coding device instead of performing the coefficient determination and storage steps before the variable length coding as recited.

Therefore, Yokoyama does not disclose a run-length converter for converting block data consisting of a plurality of image signals into combined data in accordance with a scanning sequence, each of the combined data including a number of consecutive insignificant coefficients and a value of a significant coefficient next to the consecutive insignificant coefficients as recited making the claimed invention patentably distinct and non-obvious from the cited reference.

Claim 8 is not anticipated by Fukuzawa

Claim 8 stands rejected under § 102(b) in view of Fukuzawa.

Applicant strongly contends that Fukuzawa fails to disclose the features recited in these claims such as a bit stream register for storing a received bit stream, a table memory for storing a code length of each variable length code in connection with combined data including a number of consecutive insignificant coefficients and a value of a significant coefficient next to the consecutive insignificant coefficients in accordance with a scanning sequence of block data consisting of a plurality of image signals, a data reader for reading a predetermined number of bits from said bit stream register, and an address generator for generating an address of said table memory from data read from said data reader.

In contrast, and similar to Yokoyama, Fukuzawa omits the recited feature and instead discloses a variable length decoder that uses a combination of a reverse quantizer, reverse DCT, and motion compensator to decode the encoded data to produce an image output signal. (see FIGs. 3, 4; col. 6, lines 17-32). Specifically, Fukuzawa states that "...encoded data...is supplied to a VLD (variable length decoder) 203...a quantized coefficient (quantized DCT coefficient) and quantized step width for each macroblock obtained...are supplied to a reverse quantizer 204, and a motion vector is supplied to a motion compensator 207." (see FIGs. 3, 4; col. 6, lines 17-32).

Thus, Fukuzawa does not use any table memory, data reader, and address generator as recited for variable length decoding as

instead the cited reference must use reverse quantizers and motion compensators to recover the coefficients necessary for variable length decoding. Applicant strongly contends that using a combination of motion estimators/predictors and DCT reverse processors to recover coefficients from an input encoded data as disclosed by Fukuzawa is significantly different from the recited feature of using a bit-stream register, table memory, data reader, and address generator to recover combined data, in accordance with a scanning sequence, including insignificant coefficients and a value of significant coefficients.

Furthermore, similar to Yokoyama and clearly illustrated in FIGs. 3, 4 of the cited reference, Fukuzawa teaches away from the recited invention by performing the steps of recovering/counting coefficients, storing a length of a variable length code, and performing the variable length decoding all within the variable length decoding device instead of performing the coefficient recovery and storage steps before the variable length decoding as recited.

Therefore, Fukuzawa fails to disclose a bit stream register for storing a received bit stream, a table memory for storing a code length of each variable length code in connection with combined data including a number of consecutive insignificant coefficients and a value of a significant coefficient next to the consecutive insignificant coefficients in accordance with a

scanning sequence of block data consisting of a plurality of image signals, a data reader for reading a predetermined number of bits from said bit stream register, and an address generator for generating an address of said table memory from data read from said data reader as recited making the claimed invention patentably distinct and non-obvious from the cited reference.

Conclusion

In view of the amendments and remarks submitted above, it is respectfully submitted that all of the remaining claims are allowable and a Notice of Allowance is earnestly solicited.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayments to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

The Examiner is invited to contact the undersigned at (703) 205-8000 to discuss the application.

Respectfully submitted,

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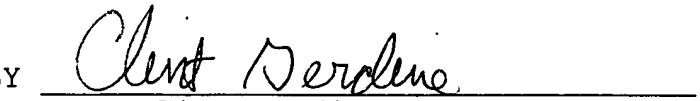
BY 

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